HTG320240A

产品名称（**Product name**）	:	单色 COG 模组
型　　号（**Model**）	:	HTG320240A
编　　号（**Part number**）	:	20161022
日　　期（**Date**）	:	2016-10-22

深圳市鑫洪泰电子科技有限公司 **Shenzhen Hot Display Technology Co.,Ltd**		
编制 **Prepared by**	审核 **Checked by**	核准 **Approved by**

编码：QR-R-011　A/0　　序号：

Rev.	Descriptions	Date
01	Prelimiay Release	2016-10-22

1. Basic Specifications

1.1 Display Specifications

1>LCD Display Mode	COG,FSTN,Transflective,Positive
2>Viewing Angle	6H
3>Driving Method	320*240 DOTS
4>Interface	4-SPI
5>Backlight:	6Pcs White LED
6>Controller/Driver	ST75320

1.2 Mechanical Specifications

1>Outline Dimension	107(L)x86(W)x5.8(H)mm(Detailed Information refer to LCM Drawing)
2>Active Area	89.58(L)x67.18(W)
3>View Area	102.2(L)x72.3(W)

2. Absolute Maximum Ratings

VSS1=VSS2=VSS3=0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1 & VDD3)	–0.3 ~ 6.0	V
Analog Power supply voltage	VDDA (VDD2)	–0.3 ~ 6.0	V
LCD Power supply voltage	VOUT	–0.3 ~ 24	V
LCD Power supply voltage	V3	–0.3 ~ 16.5	V
LCD Power supply voltage	V2, V1	–0.3 ~ 6.0	V
LCD Power supply voltage	AVDD	–0.3 ~ 6.0	V
LCD Power supply voltage	NVDD	-6.0 ~ 0.3	V
LCD Power supply voltage	MV1, MV2	-6.0 ~ 0.3	V
LCD Power supply voltage	MV3	-16.5 ~ 0.3	V
MCU Interface Input Voltage	Vin	–0.3 ~ VDDI+0.3	V
MCU Interface Output Voltage	Vout	–0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	–40 to +85	°C
Storage temperature	TSTR	–55 to +105	°C

3. Electrical Characteristics

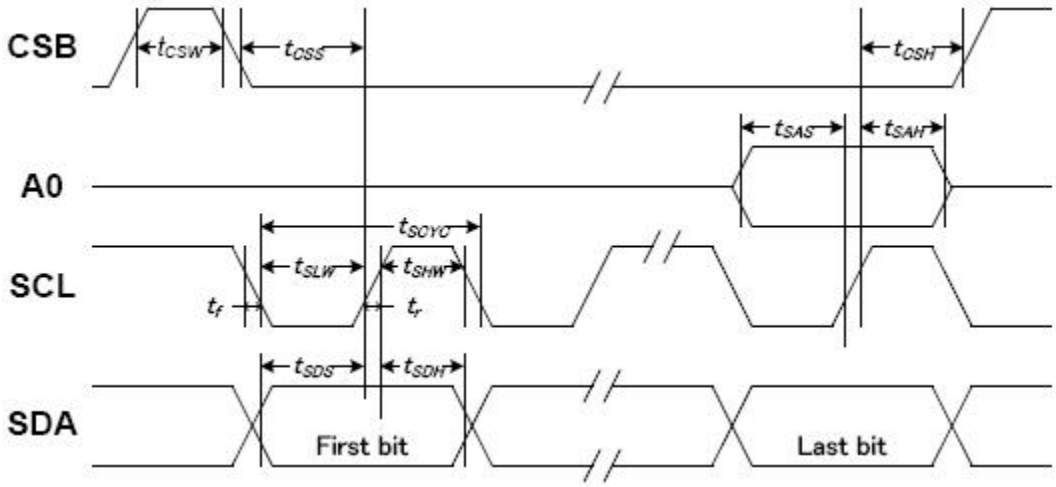
3.1 DC Characteristics

VSS1=VSS2=VSS3 =0V and Ta = –40 ~ 85 °C, unless otherwise specified.

Item	Symbol	Condition	Related Pin	Rating			Unit
				Min.	Typ.	Max.	
Digital Operating Voltage	VDDI		VDD1, VDD3	2.7	–	5.5	V
Analog Operating Voltage	VDDA		VDD2	2.7	–	5.5	V
Input High-level Voltage	V_{IH}		MCU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}		MCU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}	I_{OH}=1.0mA, VDD1=3V	D[7:0] TSYNC	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}	I_{OL}=–1.0mA, VDD1=3V	D[7:0] TSYNC	VSS1	–	0.2*VDD1	V
V3 Accuracy	ΔV3	Ta=25°C, VDD=3.0V, V3=10V, Bias=1/12	V3	-0.12	–	0.12	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1	MCU Interface	–1.0	–	1.0	μA
ON Resistance of LCD Drivers	R_{ON}	Ta=25°C, Vop=20.0V, BIAS=1/15 ΔV=10%	COM Drivers	–	1	–	KΩ
		Ta=25°C, Vop=20.0V, BIAS=1/15 ΔV=10%	SEG Drivers	–	1	–	KΩ
Operation Clock	f_{OSC}	Ta = 25°C	–	–	275	–	KHz
Vop voltage output	Vop		V3-MV3	10	-	33	V
VOUT voltage output	VOUT		VOUT	-	18	20	V

3.2 AC Characteristics

3.2.1 System Bus Timing for 4-Line SPI MCU Interface



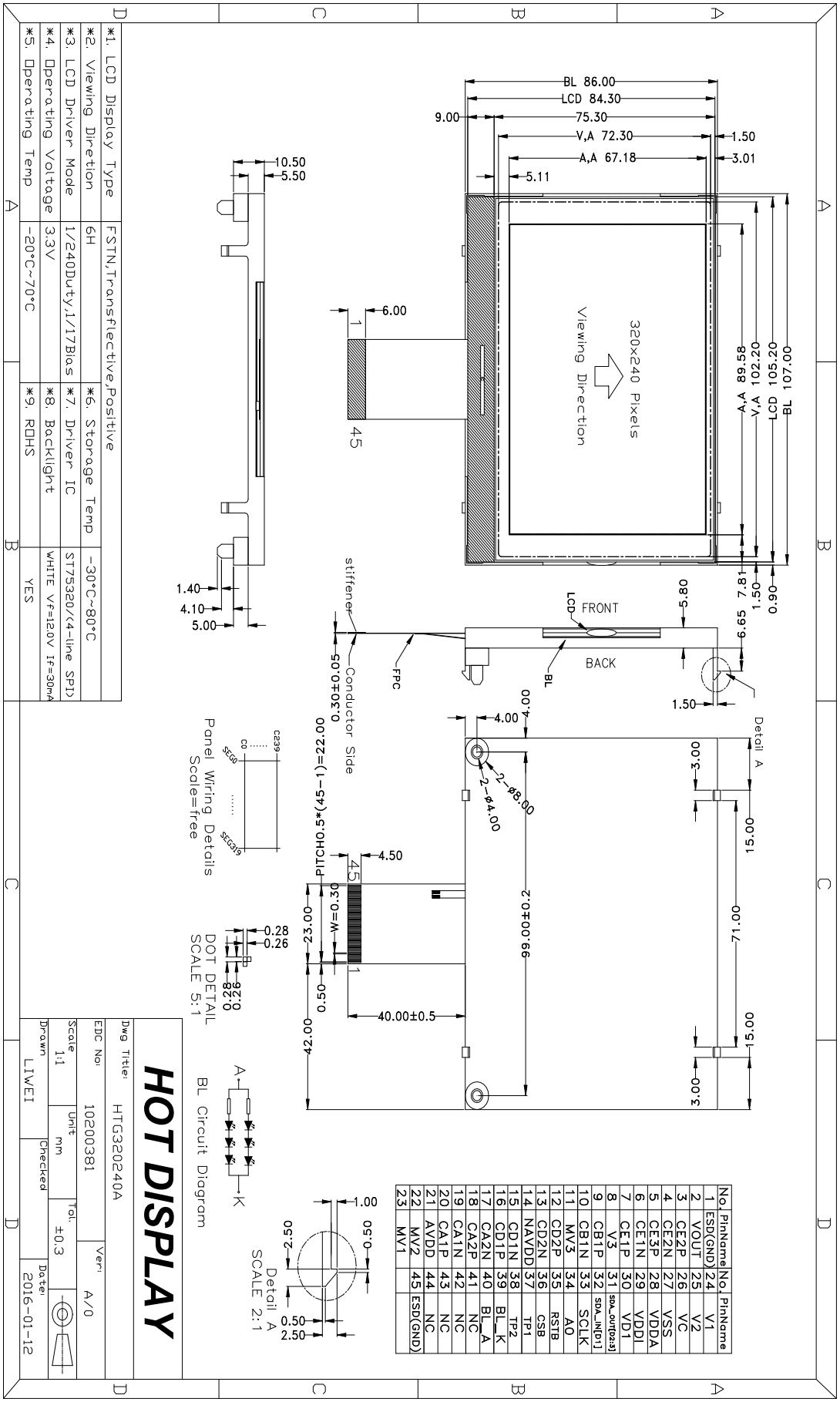
VDD1 = 3.0V~5.0V , Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		140	—	ns
SCL “H” pulse width		tSHW		70	—	
SCL “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		40	—	
Data hold time		tSDH		40	—	
CSB-SCL time	CSB	tCSS		60	—	
CSB-SCL time		tCSH		70	—	
CSB “H” pulse width		tCSW		15	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

4. Structure Block



*1. LCD Display Type	FSTN,Transflective,Positive		
*2. Viewing Direction	6H	*6. Storage Temp	-30°C~80°C
*3. LCD Driver Mode	1/240Duty,1/17Bias	*7. Driver IC	ST7532O(4-line SPI)
*4. Operating Voltage	3.3V	*8. Backlight	WHITE Vf=12.0V If=30mA
*5. Operating Temp	-20°C~70°C	*9. ROHS	YES

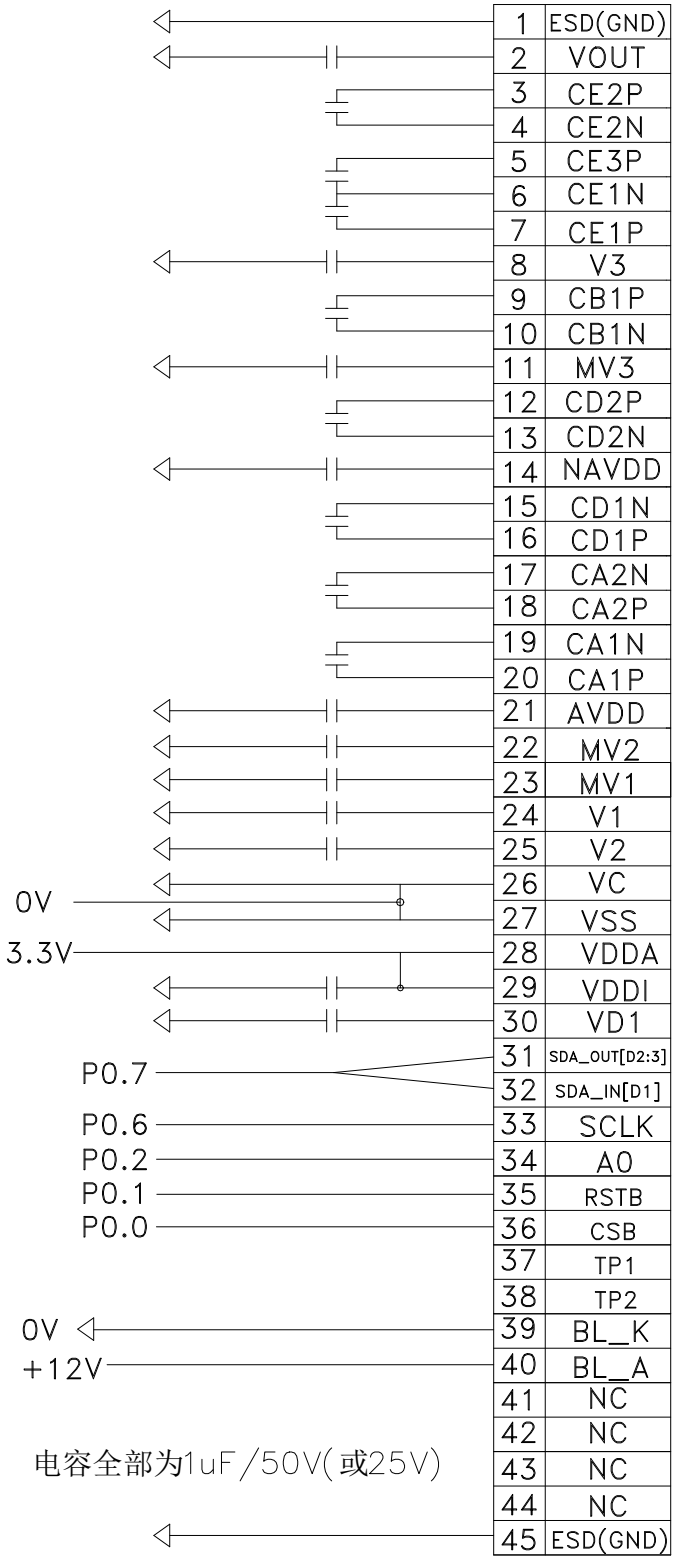
No.	PinName	No.	PinName
1	ESD(GND)	24	V1
2	VOUT	25	V2
3	CE2P	26	VC
4	CE2N	27	VSS
5	CE3P	28	VDDA
6	CE1N	29	VDDI
7	CE1P	30	VD1
8	V3	31	SDA_OUT[D2:3]
9	CB1P	32	SDA_IN[D1]
10	CB1N	33	SCLK
11	MV3	34	A0
12	CD2P	35	RSTB
13	CD2N	36	CSB
14	NAVDD	37	TP1
15	CD1N	38	TP2
16	CD1P	39	BL_K
17	CA2N	40	BL_A
18	CA2P	41	NC
19	CA1N	42	NC
20	CA1P	43	NC
21	AVDD	44	NC
22	MV2	45	ESD(GND)
23	MV1		

4.1 Terminal Function

Pin No.	Pin Name	Function
1	ESD(GND)	Frame ground.
2	VOUT	VOUT is the source of V3 regulator.
3	CE2P	Connects a non-polar capacitor between CE2P and CE2N.
4	CE2N	Connects a non-polar capacitor between CE2P and CE2N.
5	CE3P	Connects a non-polar capacitor between CE3P and CE1N.
6	CE1N	Connects a non-polar capacitor between CE3P and CE1N.
7	CE1P	Connects a non-polar capacitor between CE1P and CE1N.
8	V3	LCD driver supply.
9	CB1P	Connects a non-polar capacitor between CB1P pin and CB1N pin.
10	CB1N	Connects a non-polar capacitor between CB1P pin and CB1N pin.
11	MV3	LCD driver supply.
12	CD2P	Connects a non-polar capacitor between CD2P pin and CD2N pin.
13	CD2N	Connects a non-polar capacitor between CD2P pin and CD2N pin.
14	NAVDD	DC/DC converter for LCD driver circuit.
15	CD1N	Connects a non-polar capacitor between CD1P pin and CD1N pin.
16	CD1P	Connects a non-polar capacitor between CD1P pin and CD1N pin.
17	CA2N	Connects a non-polar capacitor between CA2P and CA2N.
18	CA2P	Connects a non-polar capacitor between CA2P and CA2N.
19	CA1N	Connects a non-polar capacitor between CA1P and CA1N.
20	CA1P	Connects a non-polar capacitor between CA1P and CA1N.
21	AVDD	DC/DC converter for LCD driver circuit.
22	MV2	LCD driver supply.
23	MV1	LCD driver supply.
24	V1	LCD driver supply.
25	V2	LCD driver supply.
26	VC	VC should be connected with ground system.
27	VSS	Power supply(0V).
28	VDDA	Power supply(3.3V).
29	VDDI	VDD1 is the power of interface I/O circuit and OSC circuit.
30	VD1	LCD driver supply.
31	SDA_OUT [D2:3]	serial output data.
32	SDA_IN [D1]	serial input data.
33	SCLK	serial input clock.
34	A0	A0 determines whether the access is related data or command.
35	RSTB	Reset input pin.
36	CSB	Chip select input pin.
37	TP1	No connect.
38	TP2	No connect.
39	BL_K	Cathode of LED backlight(0V).

40	BL_A	Anode of LED backlight(+12V).
41-44	Nc	No connect.
45	ESD(GND)	Frame ground.

4.2 Application Circuit



5. Function Description

5.1 Microprocessor Interface

When CSB is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is not active (CSB="H"), the internal shift register and counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.

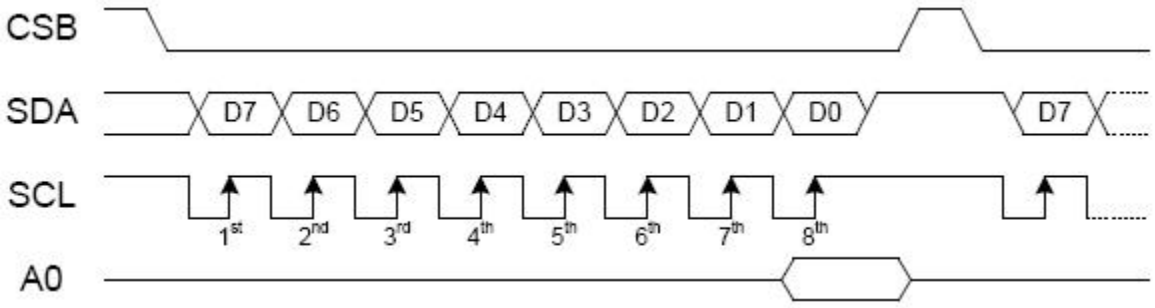


Figure 5.1 Write-Operation of 4-Line Serial Interface

5.2 Display Data RAM (DDRAM)

ST75320 containing a 320x240 bits static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 320 columns by 240 rows. When the data bit in DDRAM is "1", the segment driver will output "ON" voltage. If it is "0", the segment driver will output "OFF" voltage. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.

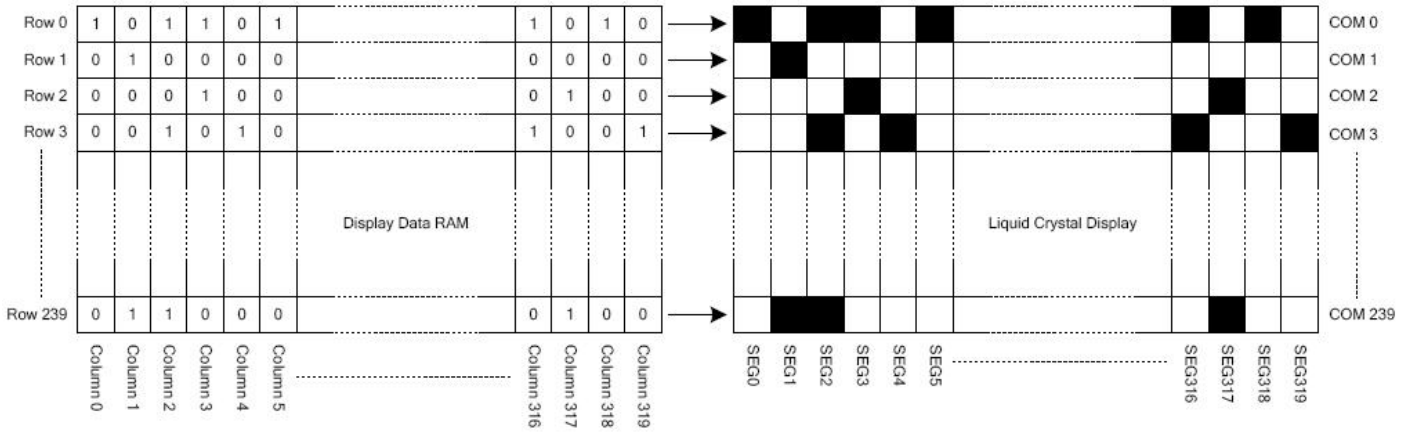


Figure 5.2.1 DDRAM Mapping

5.2.1 Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates a 6-bit Page Address Register which can be modified by the instruction of Page Address Set only. As shown in Figure 14, the 240 rows are configured as 30 pages with 8-bit. The page address must be set before accessing DDRAM content.

5.2.2 Column Address Circuit

This circuit provides the column address of DDRAM. It incorporates a 9-bit Column Address Register which can be modified by the instruction of “Column Address” only. The column address must be set before accessing DDRAM content.

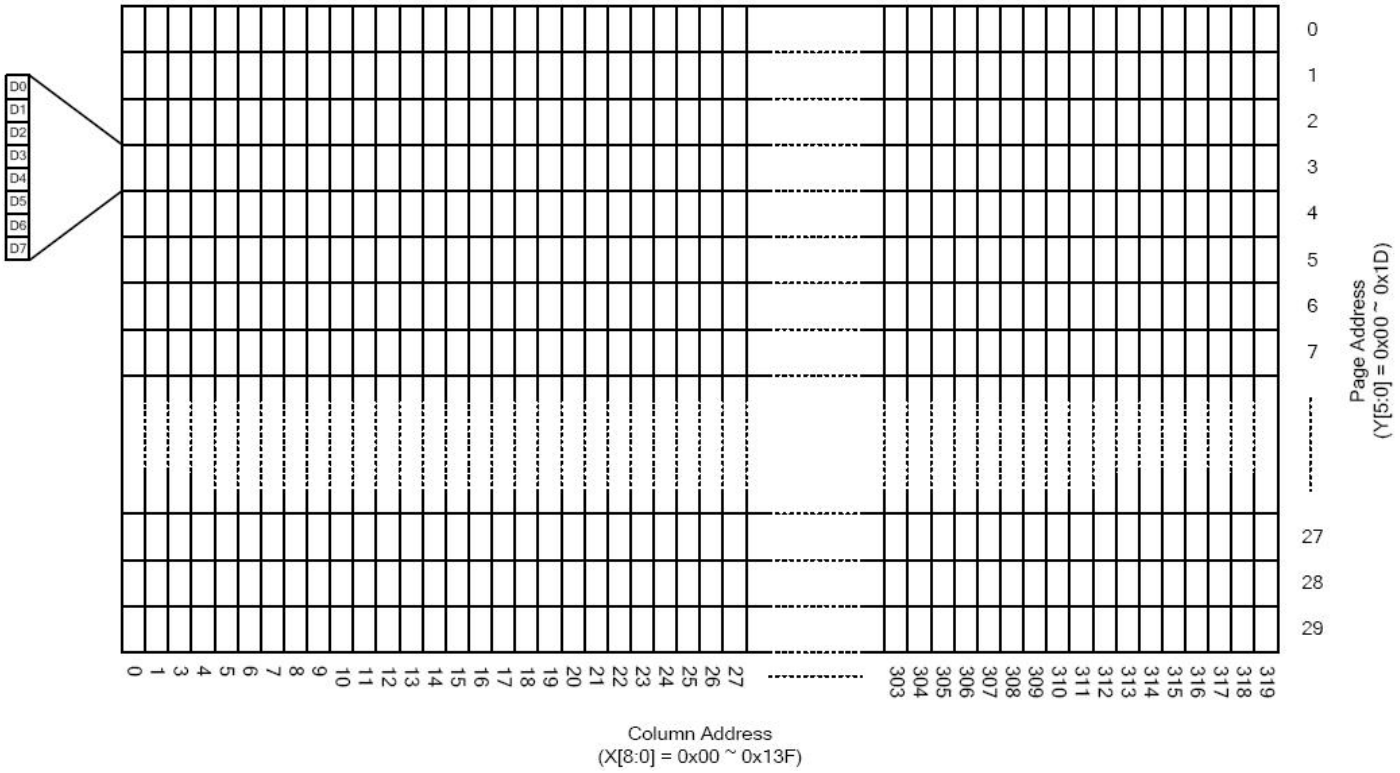


Figure 5.2.2 DDRAM Format

5.3 LCD Display Function

5.3.1 DDRAM Map to LCD Driver Output

The relation between DDRAM and outputs with different MX or MY setting is shown below.

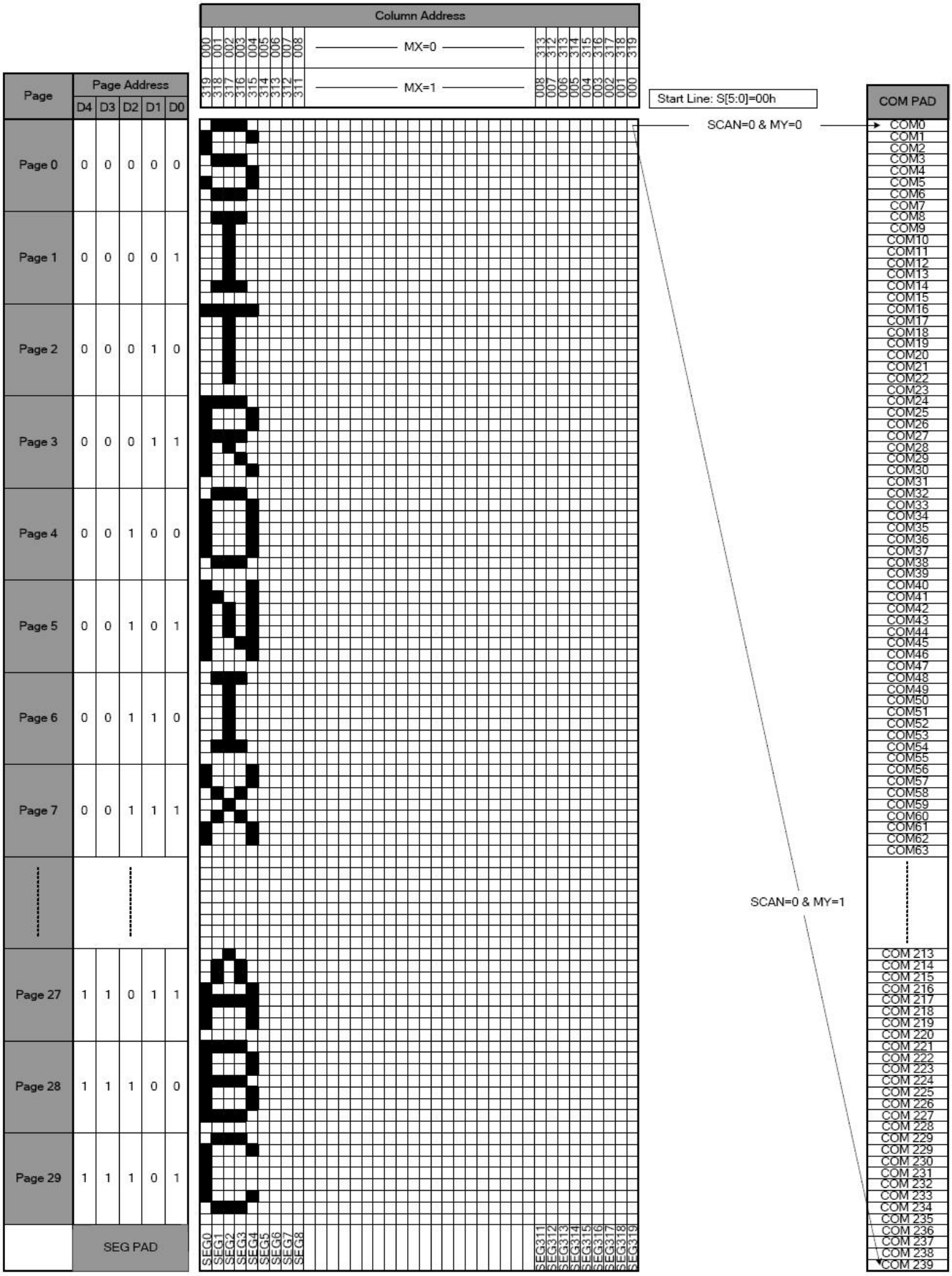


Figure 5.3.1 DDRAM Display Direction (Normal Scan)

5.3.2 Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (setting by instruction of Display Area Set) of the display. Therefore, by setting Line Address repeatedly, ST75320(LCD controller) is possible to realize the screen scrolling (4-lines basis) and page switching without changing the content of DDRAM as shown below.

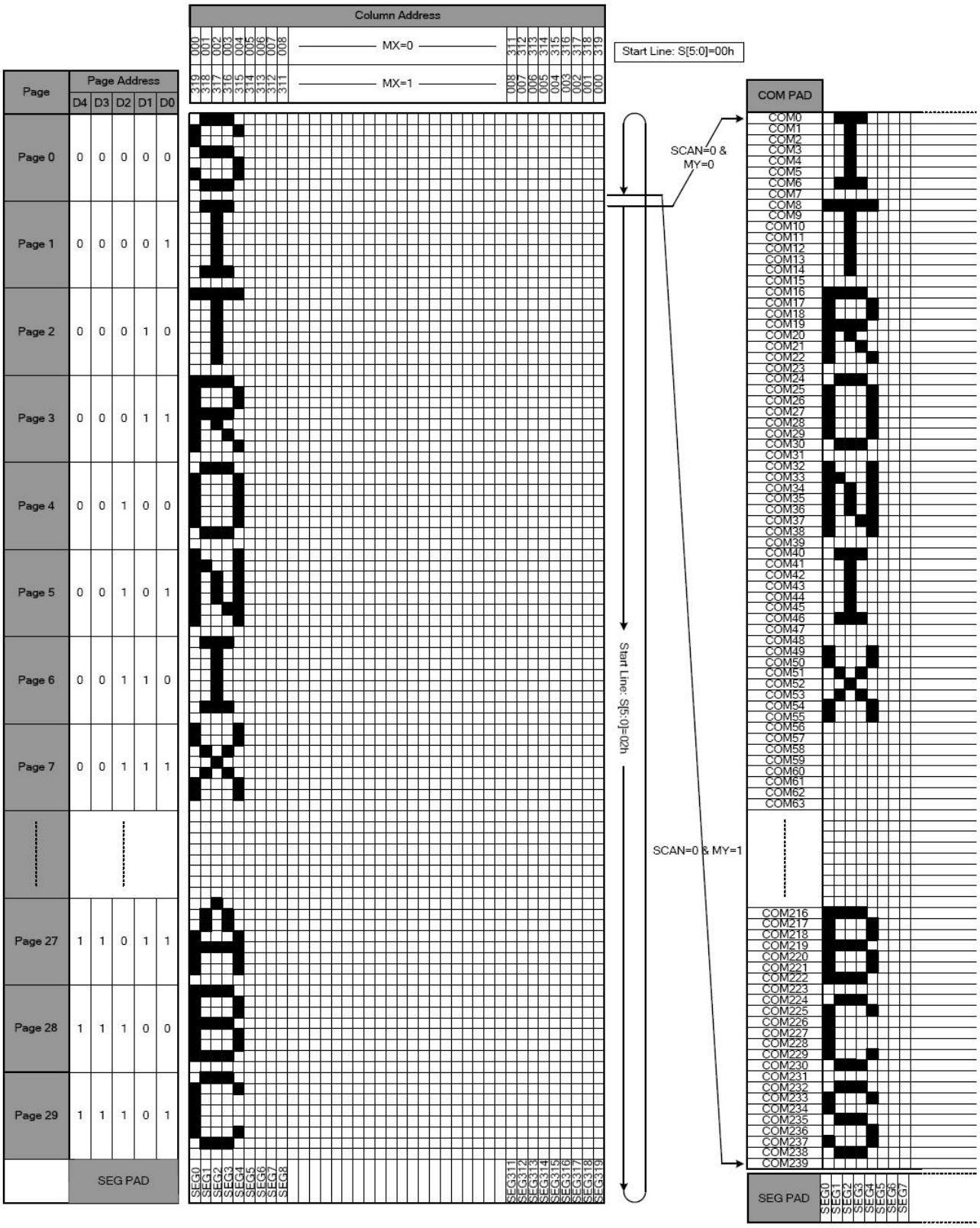


Figure 5.3.2 Display Data RAM Map (1/240 Duty)

5.4 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

5.4.1 Voltage Regulator Circuits

The internal voltage regulator circuit provides the liquid crystal operating voltage (Vop) by adjusting register (EV[9:0]). The Vop calculation formula is shown below:

Vop = V3 - MV3 = (5.0 + 0.02 x EV[9:0]) – (-5.0 - 0.02 x EV[9:0])

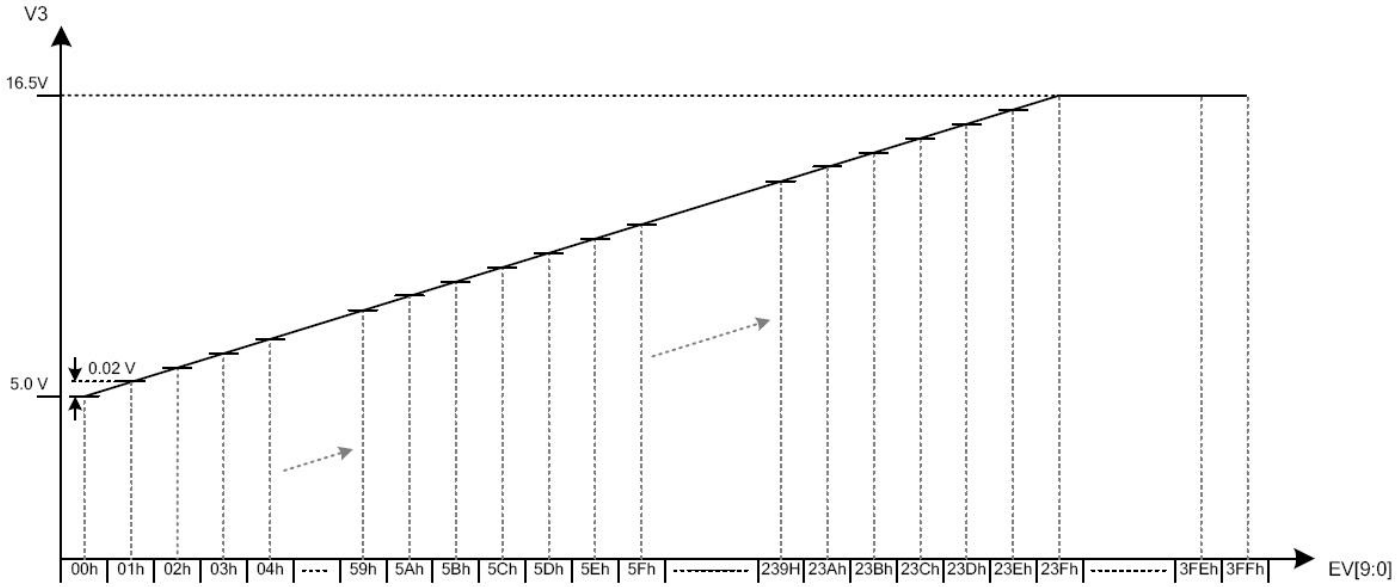


Figure 5.4.1 Vop Programmable Range

6. Command Table

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	Set LCD display mode D=0: display off D=1: display on
Display Inverse	0	0	1	0	1	0	0	1	1	INV	Set inverse display mode INV=0: normal display INV=1: inverse display
Display All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all pixel on mode AP=0: normal display AP=1: all pixel on
COM Output Status	0	0	1	1	0	0	0	1	0	0	Set COM output mode SCAN=0: normal scan SCAN=1: interlace scan MY=0: COM0→COM239 MY=1: COM239→COM0
	1	0	-	-	-	-	-	0	SCAN	MY	
Display Start Line	0	0	1	0	0	0	1	0	1	0	Set display start line
	1	0	-	-	S5	S4	S3	S2	S1	S0	
Page Address	0	0	1	0	1	1	0	0	0	1	Set the page address of DDRAM
	1	0	-	-	Y5	Y4	Y3	Y2	Y1	Y0	
Column Address	0	0	0	0	0	1	0	0	1	1	Set the column address of DDRAM
	1	0	-	-	-	-	-	-	-	X8	
	1	0	X7	X6	X5	X4	X3	X2	X1	X0	
Display Data Write	0	0	0	0	0	1	1	1	0	1	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Read	0	0	0	0	0	1	1	1	0	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Input/Output Direction	0	0	1	0	0	0	0	1	0	DIR	Set DDRAM data input direction DIR=0: column direction DIR=1: page direction
Column Address Direction	0	0	1	0	1	0	0	0	0	MX	Set column addressing direction MX=0: COL-0→ COL-319 MX=1: COL-319→ COL-0
N-Line Inversion	0	0	0	0	1	1	0	1	1	0	Set N-Line inversion
	1	0	-	-	NL5	NL4	NL3	NL2	NL1	NL0	

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
N-Line Inversion ON/OFF	0	0	1	1	1	0	0	1	0	NL	Set N-Line inversion mode NL=0:N-Line inversion off NL=1:N-Line inversion on
Display Area	0	0	0	1	1	0	1	1	0	1	Set the display area DTY[2:0]=00h~07h SP[5:0]=00h~4Fh
	1	0	-	-	-	-	-	DTY2	DTY1	DTY0	
	1	0	-	-	SP5	SP4	SP3	SP2	SP1	SP0	
Read Modify Write	0	0	1	1	1	0	0	0	0	0	Enable Read Modify Write mode
Read Modify Write End	0	0	1	1	1	0	1	1	1	0	Disable Read Modify Write mode
Built-in Oscillator Circuit ON/OFF	0	0	1	0	1	0	1	0	1	OSC	Set built-in oscillator mode OSC=0: built-in oscillator off OSC=1: built-in oscillator on
Operation Clock Frequency	0	0	0	1	0	1	1	1	1	1	Set frame rate in different temperature range
	1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
	1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	
Power Control	0	0	0	0	1	0	0	1	0	1	Set built-in power circuits on/off
	1	0	-	VOUT	VAD	V3	VPF	VMV3	VNAD	VNF	
Frame Rate Level	0	0	0	0	1	0	1	0	1	1	Set the level of frame rate
	1	0	-	-	-	-	-	-	-	DBL	
BIAS	0	0	1	0	1	0	0	0	1	0	Set the bias ratio of liquid crystal driving voltage
	1	0	-	-	-	-	BS3	BS2	BS1	BS0	
Electronic Volume	0	0	1	0	0	0	0	0	0	1	Set the V3 level for liquid crystal driving voltage
	1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
	1	0	-	-	-	-	-	-	EV9	EV8	
Power Discharge	0	0	1	1	1	0	1	0	1	0	Set power circuits discharge.
	1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	
Power Save	0	0	1	0	1	0	1	0	0	PD	Set power save mode PD=0: normal mode PD=1: standby mode

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Gradient Compensation	0	0	0	1	0	0	1	1	1	0	Set temperature gradient compensation coefficient
	1	0	MT1[3:0]				MT0[3:0]				
	1	0	MT3[3:0]				MT2[3:0]				
	1	0	MT5[3:0]				MT4[3:0]				
	1	0	MT7[3:0]				MT6[3:0]				
	1	0	MT9[3:0]				MT8[3:0]				
	1	0	MTB[3:0]				MTA[3:0]				
	1	0	MTD[3:0]				MTC[3:0]				
	1	0	MTF[3:0]				MTE[3:0]				
Temperature Gradient Compensation Flag	0	0	0	0	1	1	1	0	0	1	Set the slope of temperature gradient is positive or negative
	1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
	1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
Read Status	0	0	1	0	0	0	1	1	1	0	Read IC status
	1	1	D	OSC	AVD	V3	VFP	VMV3	VNAD	VFN	
	1	1	DISV	ITR	MY	PD	TD	NLFR	MLS	-	
Temperature Detection	0	0	0	1	1	0	1	0	0	TD	Set temperature detection mode TD=0: disable mode TD=1: enable mode
LCD Driving Method	0	0	1	1	1	0	0	1	1	1	Set LCD driving method
	1	0	0	0	0	NLFR	1	0	0	1	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Frequency Compensation Temperature Range	0	0	1	1	1	0	1	1	0	0	Set temperature range for frequency compensation
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Temperature Hysteresis Value	0	0	1	1	1	0	1	1	0	1	Set temperature hysteresis value
	1	0	-	-	THV5	THV4	THV3	THV2	THV1	THV0	
	1	0	-	-	-	-	THF3	THF2	THF1	THF0	
Current Temperature Data	0	0	1	1	1	0	1	1	1	1	Monitor current temperature
	1	1	T7	T6	T5	T4	T3	T2	T1	T0	
Read ID	0	0	1	0	0	0	1	1	1	1	Read ID value
	1	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	

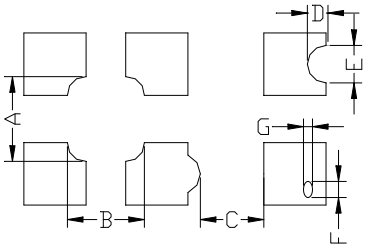
(PROM Function)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode
TE=1 & T=1											
Vop Increase	0	0	1	1	0	1	0	1	1	0	Vop increase one step
Vop Decrease	0	0	1	1	0	1	0	1	1	1	Vop decrease one step
Vop Offset	0	0	1	1	0	1	0	0	1	1	Vop offset
	1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
PROM WR/RD Control	0	0	1	0	0	1	0	0	0	1	PROM WR/RD control WR/RD=0: enable PROM read WR/RD=1: enable PROM write
	1	0	0	0	WR /RD	0	0	0	0	0	
PROM Control Out	0	0	1	0	0	1	0	0	1	0	Cancel PROM control function
PROM Write	0	0	1	0	0	1	0	0	1	1	PROM programming procedure
PROM Read	0	0	1	0	0	1	0	1	0	0	PROM up-load procedure
PROM Auto Read Control	0	0	1	0	0	1	0	1	1	0	PROM Auto Read Control XARD=0: enable auto read XARD=1: disable auto read
	1	0	0	0	0	XARD	0	0	0	0	
PROM Programming Control	0	0	1	0	0	1	1	0	0	0	PROM Programming Control EN=0 ; disable programming EN=1 ; enable programming
	1	0	0	0	0	EN	0	0	1	0	

Note:

1. "-" is disable bit. It can be either logic 0 or 1.
2. Do NOT use non-specified instructions in any extension command mode.
3. Detailed command description can refer to ST75320(LCD controller) Datasheet.

7. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2} \leq 0.28 \quad 0<C \quad \frac{D+E}{2} \leq 0.25 \quad \frac{F+G}{2} \leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor

17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

8. Handling Precautions

8.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

8.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

8.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

8.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

8.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

8.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

8.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.